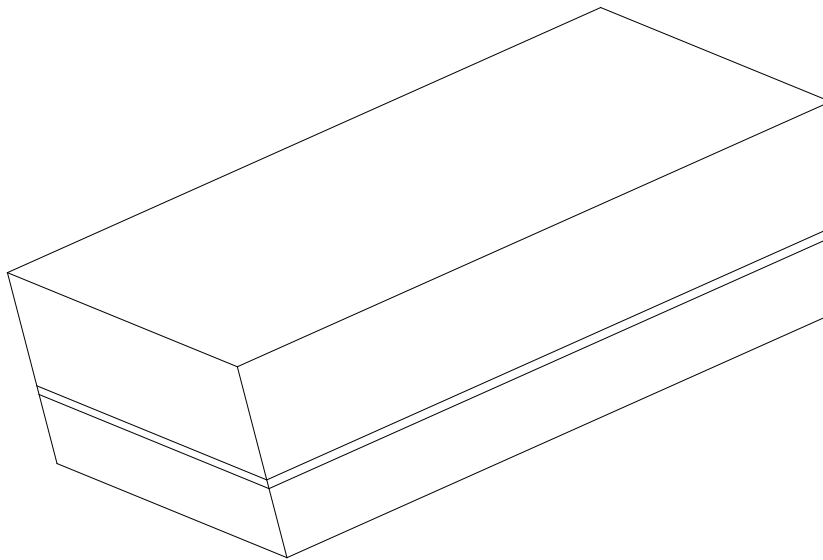


*Wooriro Splitter Chip*

**WOORIRO 2 X N SPLITTER CHIP  
SPECIFICATIONS**



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**Dimensional Parameters**

<i>Parameter</i>	-	<i>Unit</i>	<i>Nominal Value</i>	<i>Tolerance</i>
Length of PLC Chip	L	mm	Refer to page 7	$\pm 0.3$
Width of PLC Chip	W	mm	Refer to page 7	$\pm 0.2$
Thickness of PLC Chip	H	mm	2.50	$\pm 0.2$
Thickness of Substrate	T	mm	1.00	$\pm 0.05$
Thickness of adhesive	t	um	max. 50	
Width of beveling	$W_{C1}, W_{C2}$	um	max. 500	
Width of step	$W_{L1}, W_{L2}$	um	max. 200	
No. Of Output Ports	-	Ch	2~64	-
Spacing	-	um	127, 250	$\pm 0.1$
Center Spacing	-	um	Refer to page 7	$\pm 0.1$
Front Polishing Angle	$\theta_f$	degree	8	$\pm 0.3$
Side Polishing Angle	$\theta_s$	degree	90	$\pm 0.3$

Table 1. Dimensional parameters

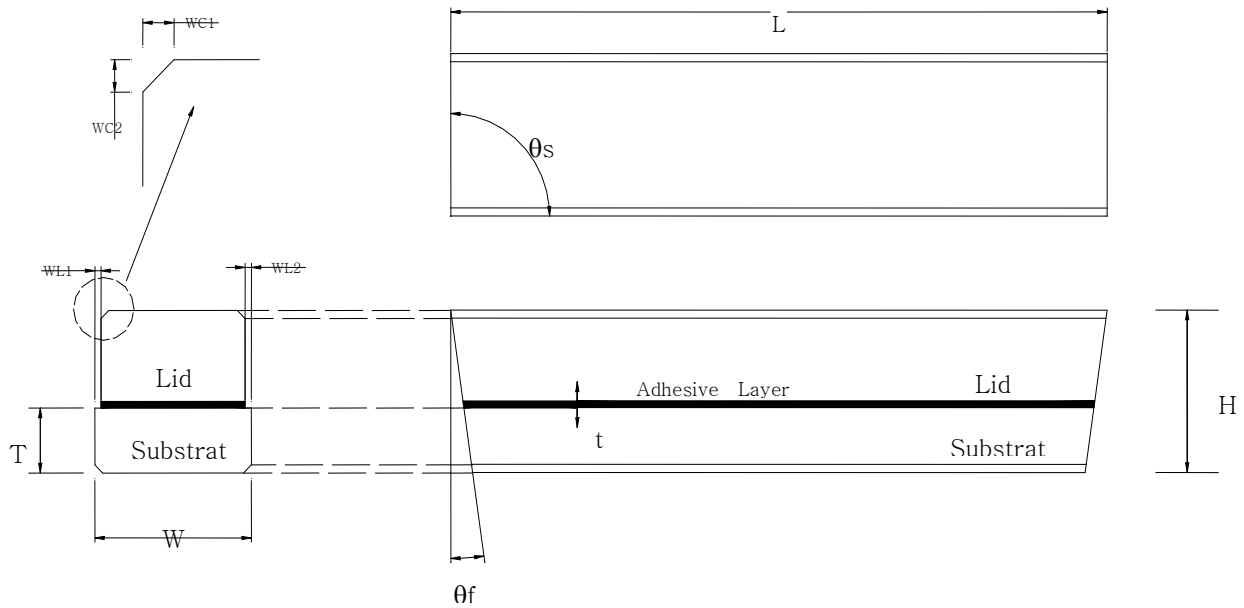



Figure 1. Dimensional parameters

Parameter and Tolerance	Figure
The distance of each input port should be 125um (Tolerance : 0) from center of chip.	

**Visual Inspection Standard Polishing Side**

**Card No: QC-WSC-1.0A**

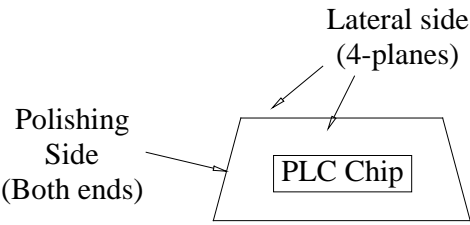
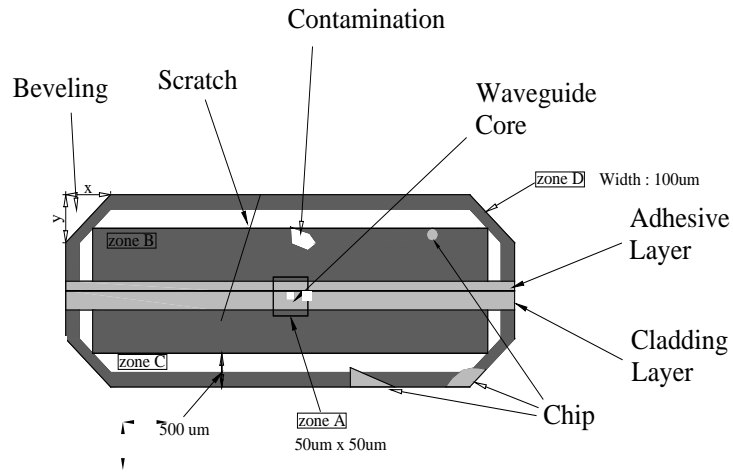
Equipment: Microscope-Magnification x50			
	Zone A	Zone B	Zone C
Scratch	Width ≤ 20um: OK Width > 20um: NG		
Chip	No visible features are allowed.	Size ≤ φ 300um up to 3pcs: OK Size > φ 300um: NG	Length > 500um: NG Width > 500um: NG Continuous chips in Zone D are excluded.
Contamination	No visible features are allowed except for which could be easily removed by ethanol		
Beveling	No visible features are allowed.		x, y ≤ 500um : OK x, y > 500um : NG

Table2. Polishing Side

### < Polishing Side (Input) >



### < Polishing Side (Output) >

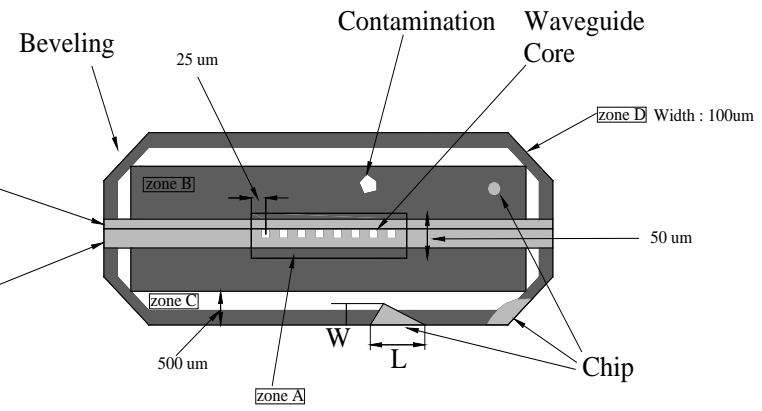


Figure 2. Polishing Side

**Visual Inspection Standard Lateral Side**

**Card No: QC-WSC-1.0B**

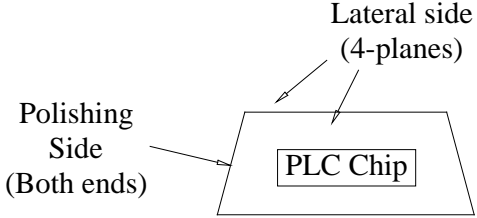
<p>Equipment: Microscope-Magnification x50</p>		 <p>Lateral side (4-planes) Polishing Side (Both ends) PLC Chip</p>
Part	Equipment	Specifications
Core & Cladding Layer	Microscope x50	<p>&lt;Crack&gt; No visible features are allowed.</p> <p>&lt;Contamination&gt; Size &gt; 500um: NG</p>
Adhesive Layer	Microscope x50	<p>&lt;Exfoliation&gt;</p> <p>No visible features are allowed on the waveguide.</p> <p>&lt;Contamination&gt;</p> <p>Size ≤ φ 500um: OK</p> <p>Size &gt; φ 500um: NG</p> <p>&lt;Bubble&gt;</p> <p>Size ≤ φ 500um: OK</p> <p>Size &gt; φ 500um: NG</p>
Surface	Eyes x1	<p>&lt;Contamination, Scratch, Crack, Chip&gt;</p> <p>&lt; Chip &gt; Length &gt; 500um : NG, Width &gt; 300um : NG</p> <p>Chipping(Defect) on backface &gt; 500um : NG</p> <p>No visible features are allowed except for beveling and scratch and which could be easily removed by ethanol cleaning.</p>

Table 3. Lateral Side

<Lateral Side>  
(Core&clading Layer)

<Lateral Side>  
(Adhesive Layer)

<Lateral Side>  
(Surface)

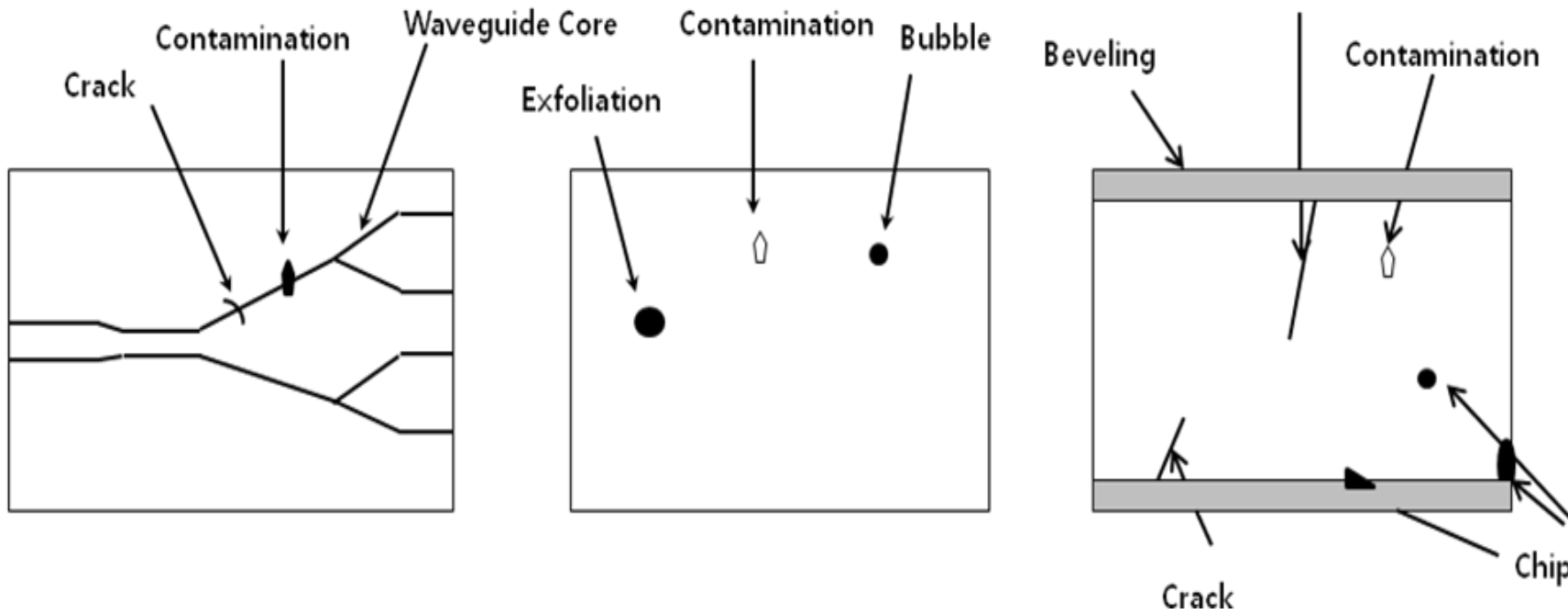


Figure 3. Lateral Side

### Wooriro Splitter Chip

Chip type	Spacing	W ( $\pm 0.2$ ) x L* ( $\pm 0.3$ ) [unit: mm]	Characteristic
2 x 2	250um	2.1 x 11.8	P1 & P2 gap: 250um (In put)
2 x 4 R1	250um	2.1 x 14.5	P1 & P2 gap: 250um (In put)
2 x 8 R1	127um	2.1 x 15.7	P1 & P2 gap: 250um (In put)
2 x 8	250um	2.6 x 17.6	P1 & P2 gap: 250um (In put)
2 x 16 R1	127um	2.6 x 18.9	P1 & P2 gap: 250um (In put)
2 x 32 R2	127um	4.6 x 23.8	P1 & P2 gap: 250um (In put)
2 x 64	127um	8.66 x 27.0	P1 & P2 gap: 250um (In put)

Table 4. Wooriro Splitter Chip

\*: Polishing angle: 98 degrees (Lid long)

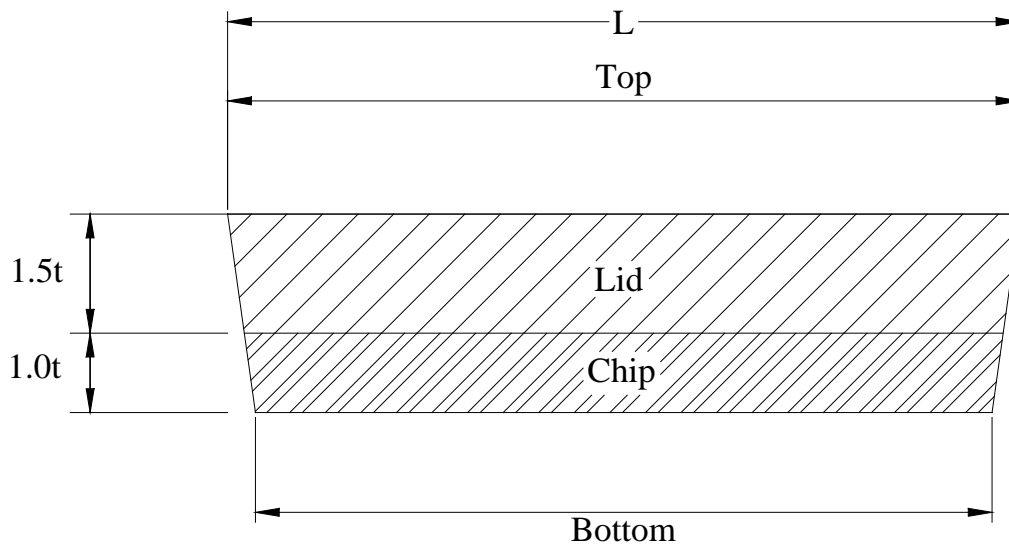


Figure 4. Wooriro splitter Chip



### Operating Conditions

<i>Parameter</i>	<i>Unit</i>	<i>Specifications</i>
Operating Temperature	°C	- 40 ~ + 85
Wavelength Range	nm	1260 ~ 1650
Maximum Input Power	mW	500

Table 5. Operating Conditions

### Optical Parameters

Model NO	WSC-2×2	WSC-2×4	WSC-2×8	WSC-2×16	WSC-2×32	WSC-2×64
N×N	2 × 2	2 × 4	2 × 8	2 × 16	2 x 32	2 x 64
Chip Level	<b>S</b>	<b>S</b>	<b>S</b>	<b>S</b>	<b>S</b>	<b>S</b>
IL (MAX)	3.7	7.1	10.3	13.5	17.0	21.0
Uni. (MAX)	0.8	1.0	1.0	1.5	1.8	2.0
PDL (MAX)	0.20	0.20	0.25	0.30	0.30	0.35
<b>S : Standard Spec</b>						

Table 6. Wooriro Splitter Chip Specification